JYOTI NIVAS COLLEGE AUTONOMOUS
SYLLABUS FOR 2018 BATCH AND THEREAFTER

Programme: B.Sc. **Semester: IV**

ELECTRONICS PAPER IV
DIGITAL ELECTRONICS AND VERILOG

Course Code: 18IVEL4 **No. of Hours: 60**

COURSES OBJECTIVES:

On completion of the following units of syllabus contents, the students must be able to:

- Understand basic logic operation of NOT, AND and OR gates with Boolean algebra. And universal property of NAND and NOR gates.
- Apply basic laws and rules of Boolean algebra and DeMorgan's theorem to Boolean expression.
- Understand Karnaugh map to simply Boolean expression and truth table function.
- Identify fixed function integrated circuits according to their complexity.
- Define propagation delay time, power dissipation, speed power product fan in and fan out in relation to logic gates.
- Discuss the logic function of the adder, subtractor, comparator, encoder, decoder, multiplexer, demultiplexer, counter and registers.
- Use full adder to implement parallel binary adders
- Implement a basic binary decoder.
- Use BCD to 7 segment decoder to display system.
- Use decoder as demultiplexer.
- Explain how RS, D, and JK flipflops differ.
- Describe the difference between an asynchronous and a synchronous counter.
- Analyze counter timing diagram and circuits.
- Determine the modulus of a counter and learn how to modify the modulus of counter.
- Use an UP/down counter to generate forward and reverse binary sequence.
- Study the structure of HDL module. Compare VHDL with HDL
- Study of Simulation and Synthesis Tools, Test Benches.
- Characteristics of Verilog and language units and types of expression.
- Analyze the gate level modeling.
- Study the data flow modeling, behavioral modeling with different examples.

COURSE OUTCOMES

- Clarify basic logic states and understand Boolean expression, Truth table and associated parameters
- Understand flip flop, counters and to modify counter
- Program using verilog and to study gate flow modulation
- Familiarize with Simulation and Synthesis Tools, Test Benches used in Digital system design
- Analyze and design combinational as well as sequential circuits

UNIT I

BOOLEAN ALGEBRA AND LOGIC FAMILIES 13HRS

Boolean algebra- Positive and negative logic. Boolean laws. De Morgan's theorems, simplification of Boolean expressions-SOP and POS. Logic gates- basic logic gates-AND, OR, NOT, logic symbol and truth table. Derived logic gates (NAND,NOR, XOR & XNOR). Universal property of NOR and NAND gates. K-map-3 and 4 variable expressions. Pulse characteristics, logic Families-classification of digital ICs. Characteristics of logic families, TTL and CMOS.Circuit description of TTL NAND gate with totem pole and open collector.
TTL IC terminology. Circuit description of CMOS inverter, comparision of TTL and CMOS families.

UNIT II

COMBINATIONAL LOGIC CIRCUITS 12 HRS

Arithmetic logic circuits: Half adder- Logic symbol, truth table and logic circuit using XOR gate and AND gate, logic circuits using NAND gates.
Full adder –logic symbol, truth table, logic diagrams (using two half adders, logic circuits using XOR gate and basic gates and logic circuits using NAND gates).
Half subtractor- logic symbol, truth table, logic circuits using XOR and basic gates and logic circuits using NAND gates.
Full subtractor- logic symbol, truth table, block diagram using two half subtractor.
4-bit parallel binary adder –Schematic block diagram, K-map simplification of all above arithmetic circuits.
Comparator: 2-bit and 4- bit Comparators, logic symbols, logic circuits using XOR and AND gates(only for 2-bit comparator),IC 7485,logic symbol, comparing two 4-bit numbers.
Decoder: basic binary decoder, 4-bit decoder, BCD to decimal decoder – logic symbol, IC 7442, truth table and applications. BCD to seven segment decoder (IC 7447), logic diagram, (common anode and common cathode), applications. Concept of zero suppression.
Driving an LCD –7 segment display format. **Encoder:** Decimal to BCD encoder, logic symbol, Decimal to BCD Priority Encoder,(IC 74LS147) truth table and applications.
Multiplexer: – 2:1,4:1,8:1 (IC 74151),logic symbol, logic circuits using basic gates, truth table, applications.
Demultiplexer: – 1:2, 1:4, 1:8 demultiplexer (IC 74154),logic symbol, logic circuits, using gates, truth table, applications.

UNIT III

SEQUENTIAL LOGIC CIRCUITS 14 HRS

Flip Flop:
Basic RS latch (NAND), clocked RS flip flop (NAND), D flip flop-logic symbol,truth table, timing diagram and working for all the flip flops.
Edge triggering and level triggering clock, asynchronous inputs.
JK flip flops using NAND gates,Race around condition, edge triggered JK flip flop, T flip flop,Master slave JK flip flop,logic symbols,logic circuits,truth table,timing diagram and working of all the flip flops.Flip flop applications.
Registers: 4-bit serial in serial out, serial in parallel out, parallel in serial out, parallel in parallel out(logic diagram,truth table,timing diagram andworking) and applications.
Counters:Asynchronous counters: 3-bit ripple counter,4-bit binary ripple counter, BCD counter,Down counters-mod 8(logic diagram,truth table and timing diagram for all the counters),Ring counter,Johnson counter.
Synchronous counter-2-bit, 3-bit Parallel binary counter,logic diagram,truth table and timing diagram.**Comparison of synchronous and asynchronous.Synchronous counter design** using K-maps for mod 3, mod 5 and decade counter.Applications of counters.
Programmable Logic devices – basic concepts.

Types of PLDs (mention only) - SPLDs–ROM, PLA, PAL and GAL.CPLD and FPGA.

UNIT IV

INTRODUCTION TO VERILOG **10HRS**

A Brief History of HDL, Structure of HDL Module, comparison of VHDL and Verilog Introduction to Simulation and Synthesis Tools, Test Benches.

Verilog: Module, Delays, brief description - data flow style, behavioral style, structural style, mixed design style, simulating design.

Language Elements: Introduction, Keywords, Identifiers, White Space Characters, Comments, format, Integers, reals and strings. Logic Values, Data Types, net types, undeclared nets, scalars and vector nets, Register type, Parameters.

Expressions: Operands, Operators, types of Expressions

Gate level modeling: Introduction, built in Primitive Gates, multiple input gates, Tri-state gates, pull gates, MOS switches, bidirectional switches, gate delay, array instances and implicit nets, Illustrative Examples (both combinational and sequential logic circuits).

UNIT V: DATA FLOW MODELING AND BEHAVIORAL MODELING **11 HRS**

Data flow Modeling: Continuous assignment, net declaration assignments, delays, net delays and examples.

Behavioral Modeling: Procedural constructs, timing controls, block statement, procedural assignments, conditional statement, loop statement, procedural continuous assignment, Illustrative Examples.

Text books:

1. Digital fundamentals:Floyd and R.P Jain –Dorling Kindersley publications,8th Edition, 2006.
2. Digital Principles and applications, Malvino and Leach –TMH 5thEdition, 2004.
3. A Verilog HDL Primer – J. Bhasker, BSP, 2008 III Edition.
4. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004 IEEE Press.

Reference Books:

1. Digital systems –Principles and applications – Ronald J. Tocci and Neal S. Widmer, PHI 8th Edition, 2005.
2. Modern Digital Electronics: R.P. Jain, 3rd edition, TMH Publications, 4th Edition, 2010.
3. Digital Design M. Morris Mano, Prentice Hall 2nd Edition, 2004.
4. Digital Fundamentals, Floyd –CBS Publications,2000.
5. Verilog and VHDL by Nazeih M Botros, 1st Edition, Charles River Media Publishers, 2005.
6. Verilog HDL, A guide to digital design and synthesis, by Samir Palnitkar, Prentice Hall, II edition, 2003.

ELECTRONICS PRACTICAL IV

List of Experiments:

Note: Minimum of 5 / 7 experiments to be performed in part A and part B.

PART A: Experiments on Digital Electronics

1. Realization of logic gates using NAND gates.
2. Construction of Half Adder and Full Adder.
3. Construction of Half Subtractor and Full Subtractor.
4. Study of Multiplexer using IC 74150 and Study of De-Multiplexer using IC 74154.
5. Clocked RS, D, JK and T FlipFlops.
6. Parallel binary adderIC 7483.
7. 4-Bit ripple counter using IC 7476 and conversion to decade counter.
8. Decimal to BCD encoder, BCD to 7 segment decoder7447.
9. Comparator: study of 4-bit magnitude comparator.
10. Decoder (2:4) using AND gates and (3:8) using IC 74138.
11. Realization of Full adder and Full subtractor using multiplexer and decoder.

Part B: Experiments on Verilog

1. Write code to realize basic and derived logic gates.
2. Half adder, Full Adderusing basic and derived gates.
3. Half subtractor and Full Subtractor using basic and derived gates.
4. Clocked D FF, T FF and JK FF (with Reset inputs).
5. Multiplexer (4x1, 8x1) and Demultiplexer using logic gates.
6. Decoder (2x4, 3x8), Encoders and Priority Encoders.
7. Design and simulation of a 4- bit Adder.
8. Code converters (Binary to Gray and vice versa).
9. 2- bit Magnitude comparator.
10. 3- bit Ripple counter.

Mini Project:

Project related to the application of digital ICs.

- Four lab units to be used for repetition, individual practice and tests.
- Four lab units to be allotted for the project.